UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/941,519	08/29/2001	William R. Wheeler	10559-605001 / P12889	6850

20985 7590 03/11/2005

FISH & RICHARDSON, PC
12390 EL CAMINO REAL
SAN DIEGO, CA 92130-2081

EXAMINER	
THOMPSON, ANNETTE M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/941,519	WHEELER ET AL.	
	Examiner	Art Unit	
	A. M. Thompson	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,4,15-17 and 38-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4 and 38-40* is/are rejected.

7)☒ Claim(s) *15-17 and 41-49* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicants' amendment to 09/941,519 has been examined. Claims 38-49 are added. Claims 5-14 and 18-37 are cancelled. Claims 1, 3, 4, 15-17, and 38-49 are pending.

2. Applicants' amendment is persuasive. However, new grounds of rejection based on Applicants' amendments are provided herein.

Specification

3. The disclosure is objected to because of the following informalities: In the specification, page 3, line 26 references the data repository as **30**. Based on Figure 1 and the specification, page 3, line 14, the data repository should be **28**.

Appropriate correction is required.

Claim Objections

4. Claims 1, 38 and 44 are objected to because of the following informalities: Pursuant to claim 1, 38 and 44, in the "monitoring a design environment" limitation, after "circuit", replace the comma with a semicolon. Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Rejection of claims 1, 3, 4, and 38-40

6. Claims 1, 3, 4, and 38-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lawman et al. (Lawman), U.S. Patent 5,673,198 in view of Applicants' admitted prior art. Lawman discloses a concurrent electronic circuit design and implementation and the limitations of independent claims 1 and 38, but fails to specifically disclose the elements of the group of integrated circuit components. Applicants' admitted prior art in the specification background discloses the components of an integrated circuit. Because lawman illustrates at least a latch and 2 NAND gates in Figure 1, it would have been obvious to one of ordinary skill in the art at the time of Applicants' invention that Lawman at least suggests the inclusion of the integrated circuit components disclosed in Applicants' admitted prior art.

7. Pursuant to claim 1, Lawman discloses a method of designing a semiconductor device (see Abstract), the method comprising: providing a plurality of component design parameter files in a data repository (Fig. 1, #20), each of the component design parameter files associated with a discrete circuitry component and including an estimated silicon area required to construct the discrete component (col. 2, ll. 27-35 references occupied area), the circuitry components including at least some components selected from the group consisting of an AND gate, an OR gate, a NAND gate, a NOR gate, an XOR gate, a latch, and a flip-flop; maintaining a circuit design parameter file (Applicants' admitted prior art in specification, page 1, lines 5-10; see also Lawman Figure 1 design window elements) for a circuit being designed (col. 2, ll. 19-29), the circuit design parameter file specifying an estimated total silicon area for the

circuit being designed (col. 2, ll. 19-39); monitoring a design environment to detect an addition of a circuitry component to the circuit (col. 2, ll. 41-56; see also col. 6, ll. 5-55); accessing a component design parameter file associated with the determined type of circuitry component that specifies the estimated silicon area required to construct the added circuitry component; (col. 2, ll. 19-39); updating the circuit design parameter file wherein updating includes adding the specified estimated silicon area required to construct the added circuitry component to the estimated total silicon area maintained in the circuit design parameter file so that the estimated total silicon area includes the silicon area required to construct the added circuitry component; and (col. 6, ll. 5-25); and providing the circuit designer with feedback concerning the estimated total silicon area required to construct the added circuitry component. (col. 6, ll. 5-25 and ll. 56-65).

8. Pursuant to claim 3, further comprising allowing the circuit designer to request feedback concerning the estimated total silicon area of the circuit being designed (col. 6, ll. 50-55).

9. Pursuant to claim 4 wherein the designer is provided with feedback concerning the estimated total silicon area of the circuit being designed in response to the circuit designer requesting feedback (col. 2, ll. 35-40; col. 2, ll. 49-56; col. 3, ll. 5-21; col. 3, ll. 24-32; col. 3, ll. 58-65; col. 9, ll. 15-29).

10. Pursuant to claims 38, 39 and 40, it comprises the limitations of claim 1, 3 and 4, respectively, but recites number of gates instead of estimated silicon area. Lawman discloses this limitation at column 9, lines 15-29, wherein it proposes an implementation process that "crosses a threshold in terms of number of gates" and further suggests that

the expert system and design library would be applicable to an embodiment utilizing feedback with "number of gates".

Allowable Subject Matter

11. Claims 15-17, 41-43 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter: Pursuant to claims 15-17 and 41-43, the prior art does not teach or suggest monitoring a design environment to detect the deletion of a circuitry component from the circuitry being designed in conjunction with providing the circuit designer with feedback concerning the total silicon area of the circuit being designed and the total number of gates of the circuit being designed. Pursuant to claims 44-49, in Applicants' method of designing a semiconductor device, the prior art does not teach or suggest providing feedback to a circuit designer regarding the number of transistors required to construct the circuit.

Conclusion

13. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications should be directed to Examiner A.M. Thompson whose telephone number is (571) 272-1909. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 4:30 p.m..

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

15. Responses to this action should be mailed to the appropriate mail stop:

Mail Stop _____
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to:

(703) 872-9306, (for all **OFFICIAL** communications intended for entry)

A. M. THOMPSON
Primary Examiner
Technology Center 2800